

Convey ThreadSim: A Simulation Framework for Latency-Tolerant Architectures

John D. Leidel
Convey Computer Corp.
jleidel@conveycomputer.com

Keywords: Hybrid-core computing, latency tolerant architecture, FPGA, graph theory, instruction set architecture, memory latency simulation

Abstract

Historically, architecture and instruction set development has been operation or function-pipe centric. In the same manner, computer architecture simulation tools have also focused on simulating the functional operations present in the target architecture/instruction set. The direct result of which are the current Von Neumann, general-purpose architectures and instruction sets that have advanced function units and poor off-core data locality. These methods work well for algorithms that exhibit low byte per operations ratios. However, this methodology is not an ideal approach for hosting latency intolerant workloads. Developing architecturally parallel platforms and instruction sets for latency intolerant workloads [such as graph theory, combinatorics and sparse matrix/vector operations] dictates that the architectural design should focus on mitigating memory operation latencies as opposed to developing complex function units. In this paper, we present a Convey-developed architecture simulation tool, ThreadSim, which simulates and records the relationship between functional architecture/instruction set parallelism and memory operation latency.